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MOTOROLA

SEMICONDUCTORS

3501 ED BLUESTEIN BLVD., AUSTIN, TEXAS 78721

MC68701

25355

Advance Information

Jameco Part Number 25355

MC68701 MICROCOMPUTER UNIT (MCU)

The MC68701 is an 8-bit single chip microcomputer unit (MCU) which significantly enhances the capabilities of the M6800 family of parts. It can be used in production systems to allow for easy firmware changes with minimum delay or it can be used to emulate the MC6801/03 for software development. It includes an upgraded M6800 microprocessor unit (MPU) with upward source and object code compatibility. Execution times of key instructions have been improved and several new instructions have been added including an unsigned multiply. The MCU can function as a monolithic microcomputer or can be expanded to a 64K byte address space. It is TTL compatible and requires one +5 volt power supply for nonprogramming operation. An additional V_{PP} power supply is needed for EPROM programming. On-chip resources include 2048 bytes of EPROM, 128 bytes of RAM, Serial Communications Interface (SCI), parallel I/O, and a three function Programmable Timer. A summary of MCU features includes:

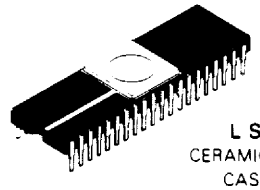
- Enhanced MC6800 Instruction Set
- 8 × 8 Multiply Instruction
- Serial Communications Interface (SCI)
- Upward Source and Object Code Compatibility with the MC6800
- 16-Bit Three-Function Programmable Timer
- Single-Chip or Expanded Operation to 64K Byte Address Space
- Bus Compatibility with the M6800 Family
- 2048 Bytes of UV Erasable, User Programmable ROM (EPROM)
- 128 Bytes of RAM (64 Bytes Retainable on Powerdown)
- 29 Parallel I/O and Two Handshake Control Lines
- Internal Clock Generator with Divide-by-Four Output
- −40 to 85°C Temperature Range

MOS

(N-CHANNEL, SILICON-GATE, DEPLETION LOAD)

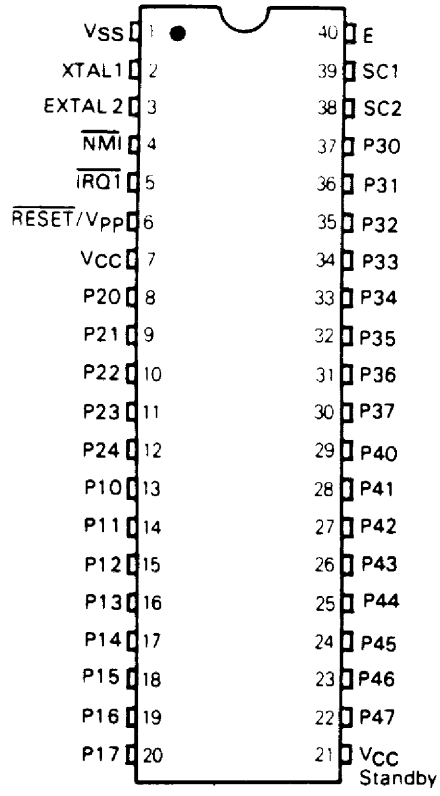
MICROCOMPUTER WITH EPROM

MOTOROLA



L SUFFIX
CERAMIC PACKAGE
CASE 715

PIN ASSIGNMENT



GENERIC INFORMATION

Package Type	Frequency (MHz)	Temperature	Generic Number
Ceramic	1.0	0°C to 70°C	MC68701L
L Suffix	1.0	−40°C to 85°C	MC68701CL
	1.25	0°C to 70°C	MC68701L-1
	1.25	−40°C to 85°C	MC68701CL-1
	1.5	0°C to 70°C	MC68A701L
	2.0	0°C to 70°C	MC68B701L

This document contains information on a new product. Specifications and information herein are subject to change without notice.

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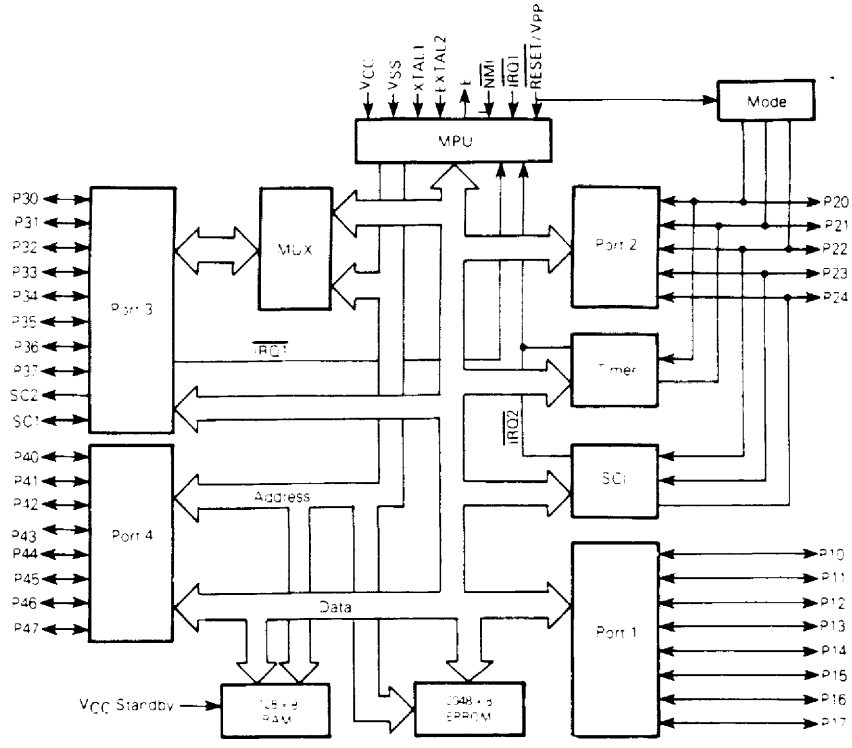
MC68701 MICROCOMPUTER BLOCK DIAGRAM



MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Supply Voltage	V_{CC}	−0.3 to +7.0	V
Input Voltage	V_{in}	−0.3 to +7.0	V
Operating Temperature Range MC68701 MC68701C	T_A	T_L to T_H 0 to 70 −40 to 85	°C
Storage Temperature Range	T_{stg}	0 to 85	°C

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \le (V_{in}$ or $V_{out}) \le V_{CC}$. Reliability of operation is enhanced if unused inputs are tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{CC}).

THERMAL CHARACTERISTICS

Characteristic	Symbol	Value	Rating
Thermal Resistance Ceramic Package	θ_{JA}	50	°C/W

POWER CONSIDERATIONS

The average chip-junction temperature, T_J, in °C can be obtained from:

$$T_J = T_A + (P_D \bullet \theta_{JA}) \quad (1)$$

Where:

T_A ≡ Ambient Temperature, °C

θ_{JA} ≡ Package Thermal Resistance, Junction-to-Ambient, °C/W

$P_D \equiv P_{INT} + P_{PORT}$

$P_{INT} \equiv I_{CC} \times V_{CC}$, Watts — Chip Internal Power

P_{PORT} ≡ Port Power Dissipation, Watts — User Determined

For most applications $P_{PORT} \ll P_{INT}$ and can be neglected. P_{PORT} may become significant if the device is configured to drive Darlington bases or sink LED loads.

An approximate relationship between P_D and T_J (if P_{PORT} is neglected) is:

$$P_D = K \div (T_J + 273°C) \quad (2)$$

Solving equations 1 and 2 for K gives:

$$K = P_D \bullet (T_A + 273°C) + \theta_{JA} \bullet P_D^2 \quad (3)$$

Where K is a constant pertaining to the particular part. K can be determined from equation 3 by measuring P_D (at equilibrium) for a known T_A. Using this value of K the values of P_D and T_J can be obtained by solving equations (1) and (2) iteratively for any value of T_A.

CONTROL TIMING (V_{CC} = 5.0 V ±5%, V_{SS} = 0, T_A = 0 to 70°C)

Characteristic	Symbol	MC68701		MC68701-1		MC68A701		MC68B701		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
Frequency of Operation	f_o	0.5	1.0	0.5	1.25	0.5	1.5	0.5	2.0	MHz
Crystal Frequency	f_{XTAL}	2.0	4.0	2.0	5.0	2.0	6.0	2.0	8.0	MHz
External Oscillator Frequency	$4f_o$	2.0	4.0	2.0	5.0	2.0	6.0	2.0	8.0	MHz
Crystal Oscillator Start Up Time	t_{rc}	–	100	–	100	–	100	–	100	ms
Processor Control Setup Time	t_{PCS}	200	–	170	–	140	–	110	–	ns

DC ELECTRICAL CHARACTERISTICS (V_{CC} = 5.0 Vdc ±5%, V_{SS} = 0, T_A = T_L to T_H, unless otherwise noted)

Characteristic		Symbol	MC68701			MC68701C			Unit
			Min	Typ	Max	Min	Typ	Max	
Input High Voltage	$\overline{RESET}$	V_{IH}	V_{SS} + 4.0	–	V_{CC}	V_{SS} + 4.0	–	V_{CC}	V
	Other Inputs*		V_{SS} + 2.0	–	V_{CC}	V_{SS} + 2.2	–	V_{CC}	
Input Low Voltage	$\overline{RESET}$	V_{IL}	V_{SS} − 0.3	–	V_{SS} + 0.4	V_{SS} − 0.3	–	V_{SS} + 0.4	V
	Other Inputs*		V_{SS} − 0.3	–	V_{SS} + 0.8	V_{SS} − 0.3	–	V_{SS} + 0.8	
Input Current, See Note (V_{in} = 0 to 2.4 V)	Port 4	I_{in}	–	–	0.6	–	–	1.0	mA
	SCI		–	–	1.0	–	–	1.6	
Input Current (V_{in} = 0 to 5.25 V)	$\overline{NMI}$, $\overline{IRQ1}$	I_{in}	–	1.5	2.5	–	1.5	5	μA
Input Current (V_{in} = 0 to 0.4 V)	$\overline{RESET}$/V_{PP}	I_{in}	–	−2.0	–	–	−2.0	–	mA
(V_{in} = 4.0 V to V_{CC})			–	–	8.0	–	–	8.0	
Hi-Z (Off State) Input Current (V_{in} = 0.5 to 2.4 V)	Ports 1, 2, and 3	I_{TSI}	–	2	10	–	2	20	μA
Output High Voltage (I_{Load} = −65 μA, V_{CC} = Min)	Port 4, SC1, SC2	V_{OH}	V_{SS} + 2.4	–	–	V_{SS} + 2.4	–	–	V
(I_{Load} = −100 μA, V_{CC} = Min)	Other Outputs		V_{SS} + 2.4	–	–	V_{SS} + 2.4	–	–	
Output Low Voltage I_{Load} = 2.0 mA, V_{CC} = Min)	All Outputs	V_{OL}	–	–	V_{SS} + 0.5	–	–	V_{SS} + 0.6	V
Darlington Drive Current (V_O = 1.5 V)	Port 1	I_{OH}	1.0	2.5	10.0	1.0	2.5	10.0	mA
Internal Power Dissipation (Measured at T_A = T_L in Steady-State Operation)		P_{INT}	–	–	1500	–	–	1500	mW
Input Capacitance (V_{in} = 0, T_A = 25°C, f_o = 1 MHz)	Port 3,	C_{in}	–	–	12.5	–	–	12.5	pF
	Port 4, SCI		–	–	12.5	–	–	12.5	
	Other Inputs		–	–	10.0	–	–	10.0	
V_{CC} Standby	Powerdown	V_{SBB}	4.0	–	5.25	4.0	–	5.25	V
	Powerup	V_{SB}	4.75	–	5.25	4.75	–	5.25	
Standby Current	Powerdown	I_{SBB}	–	–	6.0	–	–	8.0	mA
Programming Time Per Byte (T_A = 25°C)		t_{PP}	25	–	50	25	–	50	ms
Programming Voltage (T_A = 25°C)		V_{PP}	20.0	21.0	22.0	20.0	21.0	22.0	V
Programming Current (V_{RESET} = V_{PP}, T_A = 25°C)		I_{PP}	–	30	50	–	30	50	mA

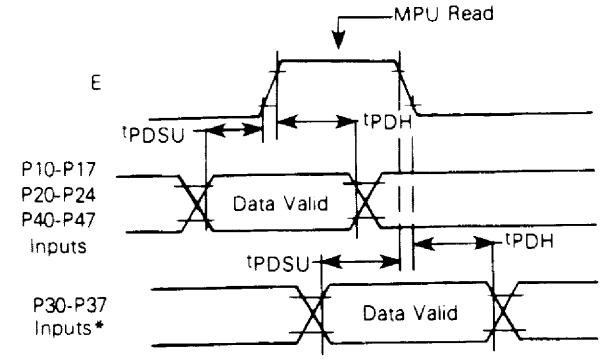
*Except mode programming levels; see Figure 15.

NOTE: $\overline{RESET}$/V_{PP} I_{in} differs from MC6801 and MC6803 values.

PERIPHERAL PORT TIMING (Refer to Figures 3-6)

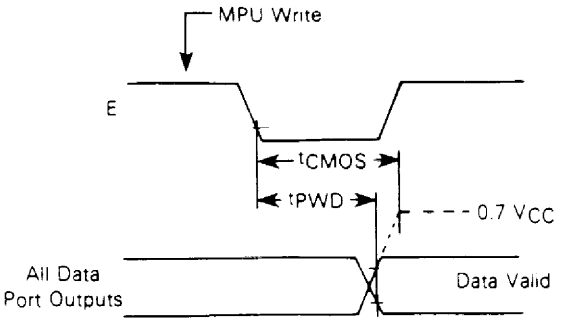
Characteristics	Symbol	MC68701		MC68701-1		MC68A701		MC68B701		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
Peripheral Data Setup Time	t_{PDSU}	200	–	200	–	150	–	100	–	ns
Peripheral Data Hold Time	t_{PDH}	200	–	200	–	150	–	100	–	ns
Delay Time, Enable Positive Transition to $\overline{OS3}$ Negative Transition	t_{OSD1}	–	350	–	350	–	300	–	250	ns
Delay Time, Enable Positive Transition to $\overline{OS3}$ Positive Transition	t_{OSD2}	–	350	–	350	–	300	–	250	ns
Delay Time, Enable Negative Transition to Peripheral Data Valid	t_{PWD}	–	350	–	350	–	300	–	250	ns
Delay Time, Enable Negative Transition to Peripheral CMOS Data Valid	t_{CMOS}	–	2.0	–	2.0	–	2.0	–	2.0	μs
Input Strobe Pulse Width	t_{PWIS}	200	–	200	–	150	–	100	–	ns
Input Data Hold Time	t_{IH}	50	–	50	–	40	–	30	–	ns
Input Data Setup Time	t_{IS}	20	–	20	–	20	–	20	–	ns

FIGURE 1 — DATA SETUP AND HOLD TIMES (MPU READ)



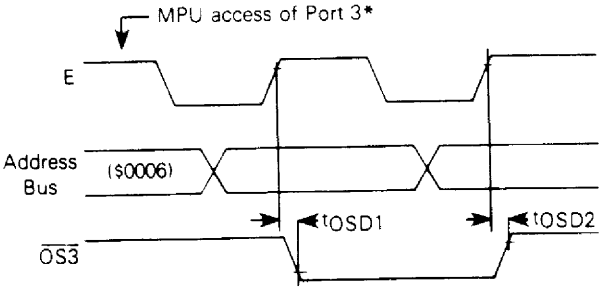
* Port 3 Non-Latched Operation (LATCHE ENABLE = 0)

FIGURE 2 — DATA SETUP AND HOLD TIMES (MPU WRITE)



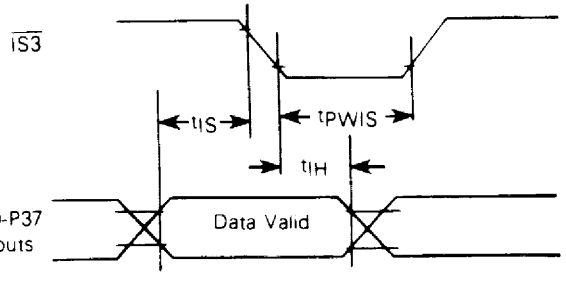
NOTES:
1. 10 k Pullup resistor required for Port 2 to reach 0.7 V_{CC}
2. Not applicable to P21
3. Port 4 cannot be pulled above V_{CC}

FIGURE 3 — PORT 3 OUTPUT STROBE TIMING (SINGLE-CHIP MODE)



* Access matches Output Strobe Select (OSS = 0, a read; OSS = 1, a write)

FIGURE 4 — PORT 3 LATCH TIMING (SINGLE-CHIP MODE)



NOTE: Timing measurements are referenced to a low voltage of 0.8 volts and a high voltage of 2.0 volts unless otherwise noted.

FIGURE 5 — CMOS LOAD

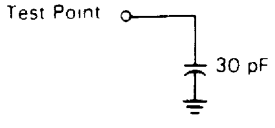
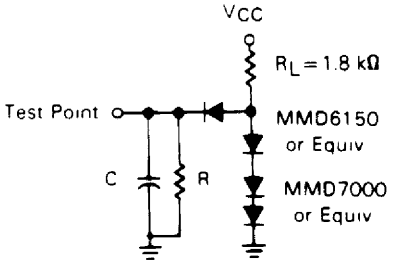


FIGURE 6 — TIMING TEST LOAD PORTS 1, 2, 3, 4



C = 90 pF for P30-P37, P40-P47, E, SC1, SC2
= 30 pF for P10-P17, P20-P24
R = 37 kΩ for P40-P47, SC1, SC2,
= 24 kΩ for P10-P17, P20-P24, P30-P37, E

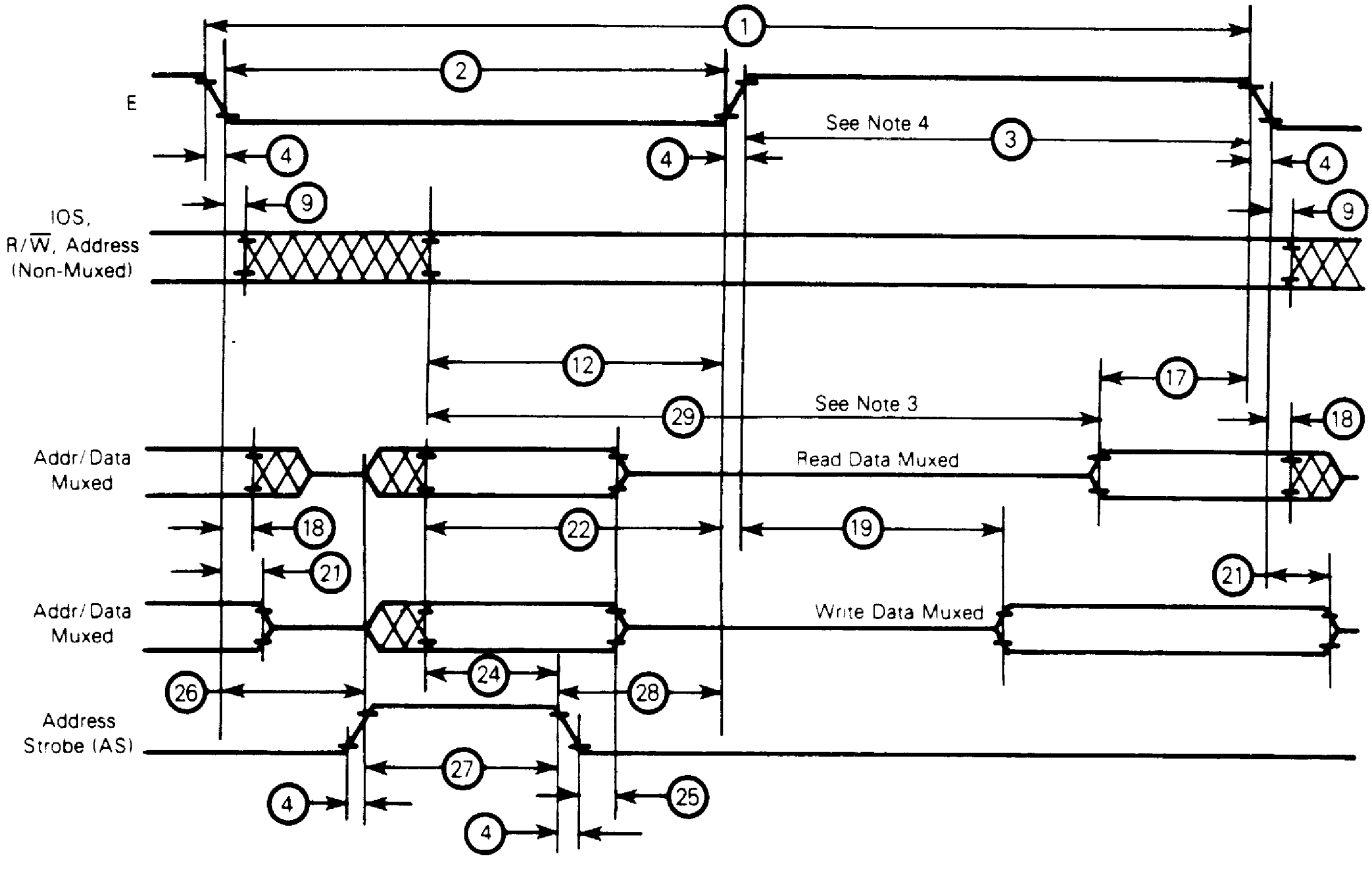
BUS TIMING (See Notes 2 and 3)

Ident Number	Characteristic	Symbol	MC68701		MC68701-1		MC68A701		MC68B701		Unit
			Min	Max	Min	Max	Min	Max	Min	Max	
1	Cycle Time	t_{cyc}	1.0	2.0	0.8	2.0	–	2.0	0.5	2.0	µs
2	Pulse Width, E Low	PW_{EL}	430	1000	360	1000	300	1000	210	1000	ns
3	Pulse Width, E High	PW_{EH}	450	1000	360	1000	300	1000	220	1000	ns
4	Clock Rise and Fall Time	t_r, t_f	–	25	–	25	–	25	–	20	ns
9	Address Hold Time	t_{AH}	20	–	20	–	20	–	10	–	ns
12	Non-Muxed Address Valid Time to E*	t_{AV}	200	–	150	–	115	–	70	–	ns
17	Read Data Setup Time	t_{DSR}	80	–	70	–	60	–	40	–	ns
18	Read Data Hold Time	t_{DHR}	10	–	10	–	10	–	10	–	ns
19	Write Data Delay Time	t_{DDW}	–	225	–	200	–	170	–	120	ns
21	Write Data Hold Time	t_{DHW}	20	–	20	–	20	–	10	–	ns
22	Multiplexed Address Valid Time to E Rise*	t_{AVM}	200	–	150	–	115	–	80	–	ns
24	Multiplexed Address Valid Time to AS Fall*	t_{ASL}	60	–	50	–	40	–	20	–	ns
25	Multiplexed Address Hold time	t_{AHL}	20	–	20	–	20	–	10	–	ns
26	Delay Time, E to AS Rise*	t_{ASD}	90**	–	70**	–	60**	–	45**	–	ns
27	Pulse Width, AS High*	PW_{ASH}	220	–	170	–	140	–	110	–	ns
28	Delay Time, AS to E Rise*	t_{ASED}	90	–	70	–	60	–	45	–	ns
29	Usable Access Time*	t_{ACC}	595	–	465	–	380	–	270	–	ns

*At specified cycle time.

**t_{ASD} parameters listed assume external TTL clock drive with 50% ±5% duty cycle. Devices driven by an external TTL clock with 50% ±1% duty cycle or which use a crystal have the following t_{ASD} specification: 100 nanoseconds minimum (1.0 MHz devices), 80 nanoseconds minimum (1.25 MHz devices), 65 nanoseconds minimum (1.5 MHz devices), 50 nanoseconds minimum (2.0 MHz devices).

FIGURE 7 — BUS TIMING



NOTES:

1. Voltage levels shown are $V_L \leq 0.5$ V, $V_H \geq 2.4$ V, unless otherwise specified.
2. Measurement points shown are 0.8 V and 2.0 V, unless otherwise specified.
3. Usable access time is computed by 12 + 3 − 17 + 4.
4. Memory devices should be enabled only during E high to avoid port 3 bus contention.

INTRODUCTION

The MC68701 is an 8-bit monolithic microcomputer which can be configured to function in a wide variety of applications. The facility which provides this extraordinary flexibility is its ability to be hardware programmed into eight different operating modes. The operating mode controls the configuration of 18 of the 40 MCU pins, available on-chip resources, memory map, location (internal or external) of interrupt vectors, and type of external bus. The configuration of the remaining 22 pins is not dependent on the operating mode.

Twenty-nine pins are organized as three 8-bit ports and one 5-bit port. Each port consists of at least a Data Register and a write-only Data Direction Register. The Data Direction Register is used to define whether corresponding bits in the Data Register are configured as an input (clear) or output (set).

The term "port," by itself, refers to all of the hardware associated with the port. When the port is used as a "data port" or "I/O port," it is controlled by the port Data Direction Register and the programmer has direct access to the port pins using the port Data Register. Port pins are labled as Pij where i identifies one of four ports and j indicates the particular bit.

The Microprocessor Unit (MPU) is an enhanced MC6800 MPU with additional capabilities and greater throughput. It is upward source and object code compatible with the MC6800. The programming model is depicted in Figure 8 where Accumulator D is a concatenation of Accumulators A and B. A list of new operations added to the M6800 instruction set are shown in Table 1.

The basic difference between the MC6801 and the MC68701 is that the MC6801 has an onboard ROM while the MC68701 has an onboard EPROM. The MC68701 is pin and code compatible with the MC6801 and can be used to emulate the MC6801, allowing easy software development using the onboard EPROM. Software developed using the MC68701 can then be masked into the MC6801 ROM.

In order to support the onboard EPROM, the MC68701 differs from the MC6801 as follows:

(1) Mode 0 in the MC6801 is a test mode only, while in the MC68701 Mode 0 is also used to program the onboard EPROM and has interrupt vectors at $BFF0-$BFFF rather than $FFF0-$FFFF.

(2) The MC68701 RAM/EPROM Control Register has two bits used to control the EPROM in Mode 0 that are not defined in the MC6801 RAM Control Register.

(3) The $\overline{\text{RESET}}$/Vpp pin in the MC68701 is dual purpose, used to supply EPROM power as well as to reset the device; while in the MC6801 the pin is called $\overline{\text{RESET}}$ and is used only to reset the device.

FIGURE 8 — MC68701/6801/6803 PROGRAMMING MODEL